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Question Paper Code : 77114

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2015.

Third Semester

Electronics and Communication Engineering

EC 6304 — ELECTRONIC CIRCUITS — I

(Regulation 2013)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List out the importance of selecting the proper operating point.

2. Draw a DC load line of the circuit shown in Figure 1.

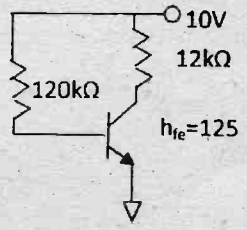

Figure 1

3. Define CMRR of BJT differential amplifier. How to improve it?

4. A small signal source $V_i(t) = 20\cos 20t + 30\sin 10^6 t$ is applied to a transistor amplifier as shown in Figure 2. The transistor has $h_{fe} = 150$, $r_0 = \infty$ and $r_\pi = 3\ \text{k}\Omega$. Determine $V_0(t)$.

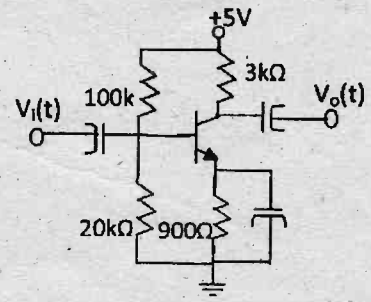

Figure 2

5. Determine the output impedance of a JFET amplifier shown in Figure 3. Let $g_m = 2$ mA/V and $\lambda = 0$.

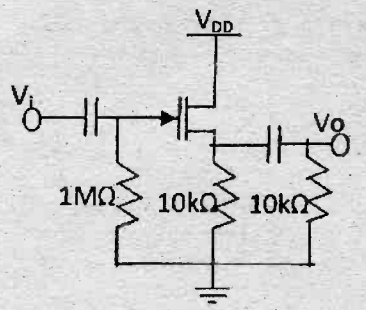

Figure 3

6. Compare between JFET and MOSFET amplifiers.

7. Find the unity gain bandwidth of MOSFET whose $g_m = 6$ mA/V, $C_{gs} = 8$ pF, $C_{gd} = 4$ pF and $C_{ds} = 1$ pF.

8. The ac schematic of an NMOS common-source stage is shown in the Figure-4, where part of the biasing circuits has been omitted for simplicity. For the N-channel MOSFET M_1, the transconductance, $g_m = 1$ mA/V, and body effect and channel length modulation effect are to be neglected. Find the lower cutoff frequency.

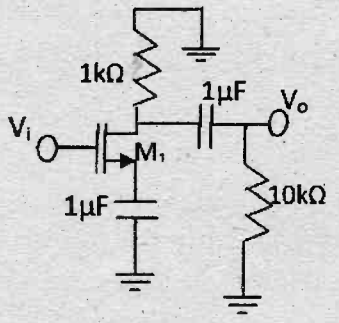

Figure-4

9. Compare NMOS amplifier with enhancement, depletion and resistive load.

10. List out the advantages of CMOS differential amplifier over MOS differential amplifier.

PART B — (5 × 16 = 80 marks)

11. (a) (i) The parameters for each transistor in the circuit in Figure-5, are $h_{fe} = 100$ and $V_{BE_{on}} = 0.7$ V. Determine the Q-point values of base, collector and emitter currents in Q_1 and Q_2. (8)

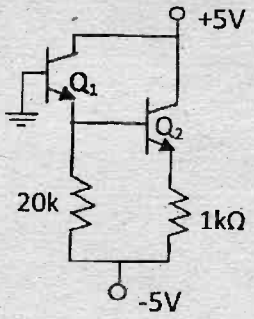

Figure 5

(ii) Determine the change in collector current produced in each bias referred to in Figures 6(a) and 6(b), when the circuit temperature raised from 25°C to 105°C and $I_{CBO} = 15$ nA @ 25°C. (8)

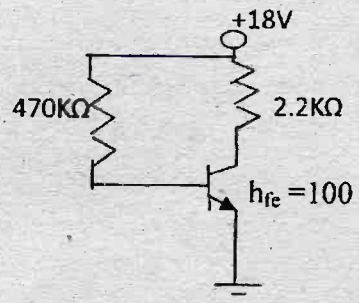

Figure 6(a)

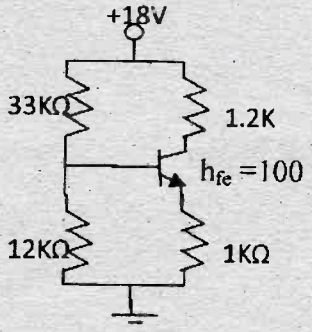

Figure 6(b)

Or

(b) (i) Determine the quiescent current and voltage values in a p-channel JFET circuit (Vide Figure-7). (6)

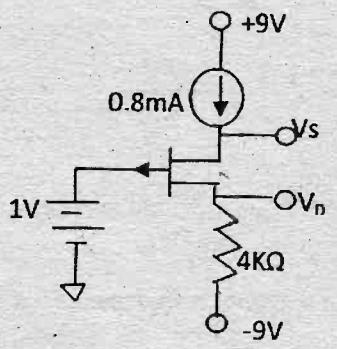

Figure-7

(ii) The circuit in Figure 8, let $h_{fe} = 100$. (1) Find V_{TH} and R_{TH} for the base circuit. (2) Determine I_{CQ} and V_{CEQ}. (3) Draw the DC load line. (10)

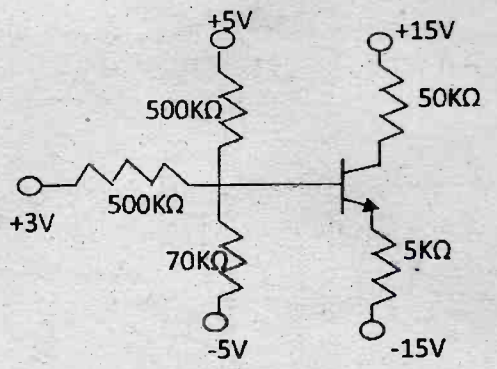

Figure 8

12. (a) (i) Consider the circuit shown in Figure-9 with the parameters are $h_{fe} = 120$ and $V_A = \infty$. (1) Determine the current gain, voltage gain, input impedance and output impedance. (2) Find the maximum undistorted output voltage swing. (12)

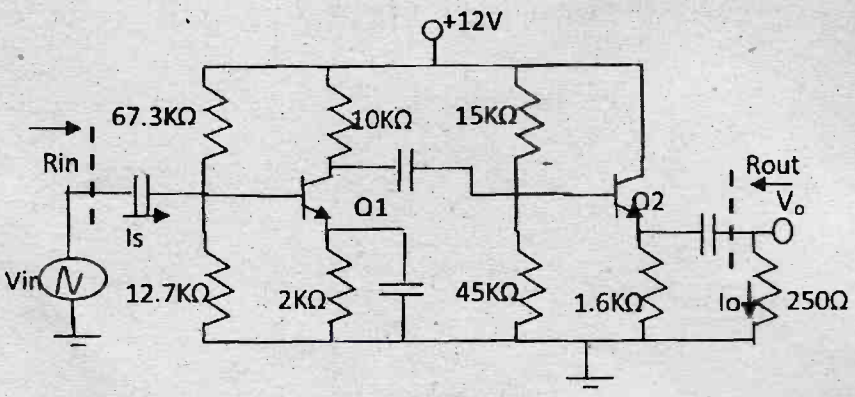

Figure 9

(ii) The parameters for each transistor in the circuit in Figure-10 are $h_{fe} = 100$, $V_A = \infty$ and $V_{BE(on)} = 0.7$ V. Determine the input and output impedances. (4)

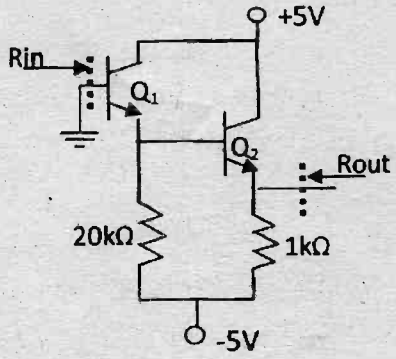

Figure 10

Or

(b) (i) For the circuit shown in Figure-11, the transistor parameters are $h_{fe} = 125$, $V_A = \infty$, $V_{CC} = 18$ V, $R_L = 4$ kΩ, $R_E = 3$ kΩ, $R_C = 4$ kΩ, $R_1 = 25.6$ kΩ and $R_2 = 10.4$ kΩ. The input signal is a current source. Determine its small signal voltage gain, current gain, maximum voltage gain and input impedance. (10)

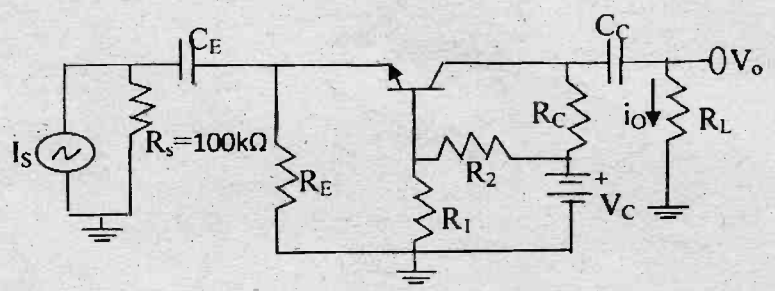

Figure 11

(ii) Draw the circuit diagram of bootstrapped emitter follower with its equivalent circuit, derive for its input and output impedance. (6)

13. (a) (i) Derive the voltage gain of BiMOS cascode amplifier shown in Figure 12. (10)

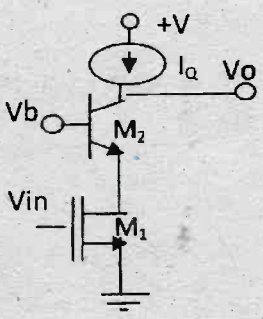

Figure 12

(ii) Draw a discrete common gate JFET amplifier and derive voltage gain, A_V, Input impedance, R_{in} and output impedance, R_{out} with small signal equivalent circuit. (6)

Or

(b) (i) Consider the PMOS amplifier shown in Figure-13. The transistor parameters are $V_{tp} = -1$ V, $\beta_p = (\mu_p Cox(W/L)) = 1$ mA/V^2 and $\lambda = 0$. (1) Determine R_D and R_S, such that $I_{DQ} = 0.75$ mA and

$V_{SDQ} = 6$ V. (2) Determine Input impedance R_i and Output impedance R_o. (3) Voltage gain, Current Gain and Maximum Output Voltage Swing. (12)

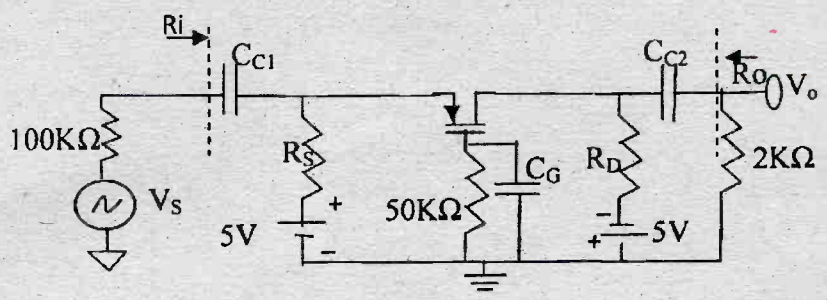

Figure-13

(ii) Determine the current gain of JFET source follower amplifier. (4)

14. (a) (i) For the circuit shown in Figure 14, let $V_{DD} = V_{SS} = 1.5$ V, $V_{tn} = 0.6$ V, $V_{tp} = -0.6$ V, all channel lengths = 1 μm, $K_n = 200\ \mu A/V^2$, $K_p = 80\ \mu A/V^2$ and $\lambda = 0$. For $I_{ref} = 10\ \mu$A, find the widths of all transistors to obtain $I_2 = 60\ \mu$A, $I_3 = 20\ \mu$A and $I_5 = 80\ \mu$A. It is further required that the voltage at the drain of Q_2 be allowed to go down within 0.2 V of the negative supply and voltage at the drain of Q_5 be allowed to go up to within 0.2 V of the positive supply. (10)

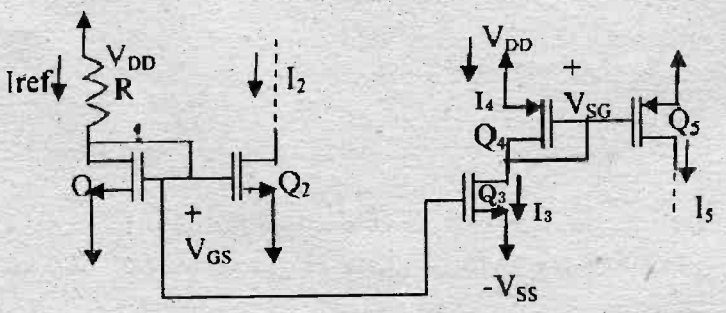

Figure-14

(ii) For the NMOS inverter circuit with saturated load (vide Figure-15), the transistor parameters are: (device data for M_D: $V_{tn_D} = 1$ V, $K_{n_D} = \mu_n Cox(W/L) = 100\ \mu A/V^2$, $\lambda_{n_D=0}$ and device data for M_L:

$V_{tn_L} = 1$ V, $K_{n_L} = \mu_n Cox(W/L) = 20\ \mu A/V^2$ and $\lambda_{n_L} = 0$). Draw its voltage-transfer characteristics curve, and mark down its transition points. (4)

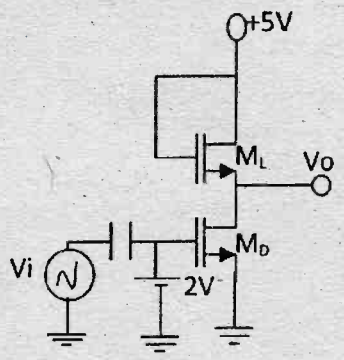

Figure-15

(iii) For CMOS differential amplifier with NMOS differential pair and PMOS current source as active load. Given $I_{DQ} = 500\ \mu A$, $(W/L)_{NMOS} = 5$, $\mu_n C_{ox} = 115\ \mu A/V^2$, $\mu_p C_{ox} = 30\ \mu A/V^2$, $\lambda_n = 0.01\ V^{-1}$, $\lambda_p = 0.02\ V^{-1}$. Find differential mode voltage gain. (2)

Or

(b) (i) Consider the circuit of NMOS amplifier with depletion load (Vide Figure-16). The transistor parameters are $V_{TND} = 0.8$ V, $V_{TNL} = -1.2$ V, $\beta_{nD} = (\mu_{nD} C_{ox}(W/L)) = 500\ \mu A/V^2$, $\beta_{nL} = (\mu_{nD} Cox(W/L)) = 50\ \mu A/V^2$, $I_{DQ} = 100\ \mu A$, $V_{DD} = 5$ V and $\lambda_{nD} = \lambda_{nL} = 0.01\ V^{-1}$. (1) Determine V_{GS} such that the Q-point is the mid of the saturation region. (2) Calculate Q-point drain current. (3) Determine the small signal voltage gain. (8)

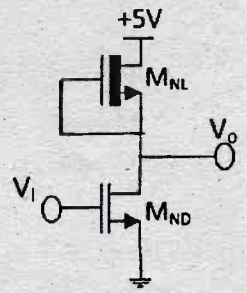

Figure-16

(ii) Determine the voltage gain, input impedance, output impedance of CMOS source follower amplifier. (8)

15. (a) (i) Derive for f_β and f_α. (6)

(ii) For the circuit shown in Figure-17 has following parameters: $h_{fe} = 125$, $C_\pi = 24$ pF, $C_\mu = 3$ pF. (1) Determine its mid-band gain, upper-cut off frequency. (2) Find the value of C_{C1}, C_{C2} and C_E by assuming lower cut-off frequency of 100 Hz. (10)

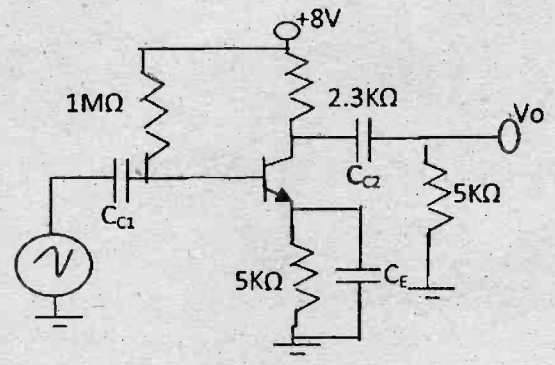

Figure-17

Or

(b) For the circuit shown in Figure-18, the NMOS transistor parameters are: $\mu_n Cox(W/L) = 2$ mA/V^2, $V_{GSQ} = 3.25$ V, $V_{tn} = 2$ V, $\lambda = 0$, $C_{gd} = 0.1$ pF and $C_{gs} = 1$ pF. Assume $C_G = C_D = C_S = 1$ pF. Calculate the mid-band gain, input impedance, output impedance, bandwidth and maximum output voltage swing. (16)

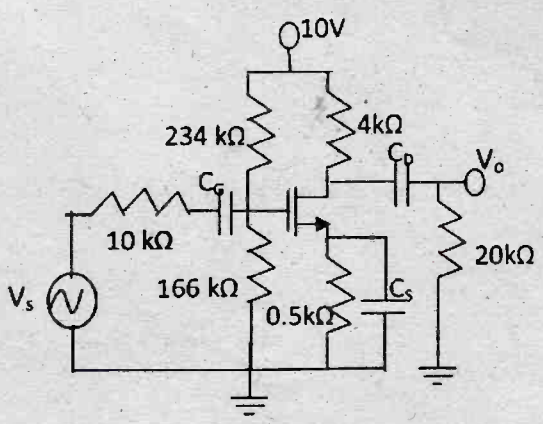

Figure-18